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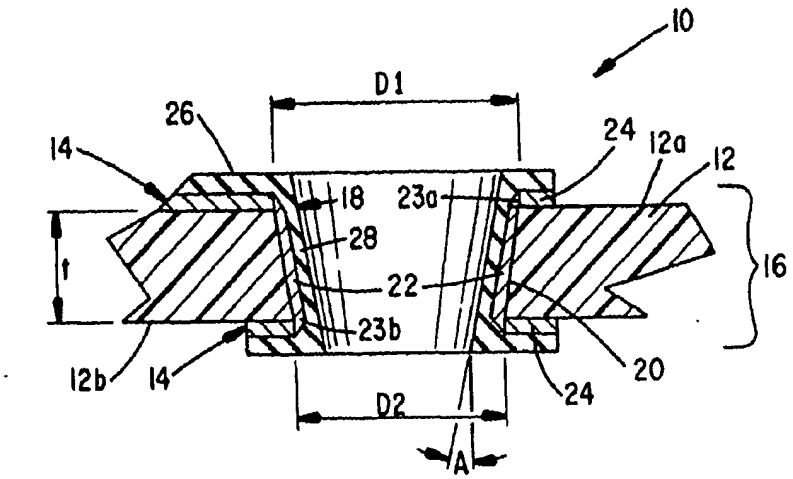
(54) Title: MULTI-METAL LAYER CIRCUIT



(57) Abstract: A circuit (10) includes a dielectric substrate (12) having two spaced apart major surfaces (12a, 12b). A first conductive layer (14) is formed on each major surface (12a, 12b) of the dielectric substrate (12). The first conductive layers (14) and the dielectric substrate (12) define a composite base substrate (16) having a tensile modulus at least 2 times greater than the tensile modulus of the dielectric substrate (12). A via (18) including a sidewall (20) extends through the composite base substrate (16). The via (18) defines edge portions (23a, 23b) in the composite base substrate (16). The edge portions (23a, 23b) of the via (18) have respective diameters less than 50 micrometers and define a via taper angle (A) less than 25 degrees. Each first conductive layer (14) is patterned to define a perimeter of a capture pad (24) encompassing the via (18). The perimeter of each capture pad (24) has a diameter less than 150 micrometers. A conductive seed layer (22) is formed on the sidewall (20) of the via (18). A second conductive layer (28) is formed contiguously on each first conductive layer (14) and on the seed layer (22).

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MULTI-METAL LAYER CIRCUIT

Field of the Invention

The invention disclosed herein relates generally to printed circuits. More specifically, the invention relates to multi-metal layer flexible circuits having microvia constructions.

Background of the Invention

A typical two metal circuit construction includes patterned conductive features on opposing surfaces of a dielectric substrate. Conductive vias electrically connect the conductive features of one surface with one or more conductive feature on the other surface for communicating electrical signals through the dielectric substrate. Typically, two metal circuit constructions allow for higher circuit densities per unit area than single metal circuits. Higher circuit densities are desirable in high performance applications.

Conventional two metal layer flex circuits are typically constructed with either plated through hole (PTH) vias or blind vias. A PTH via is a metallized hole that extends completely through opposing surfaces of a metallized dielectric substrate. PTH vias are typically formed using mechanical drilling, laser ablation or chemical etching techniques followed by a suitable metal deposition process. Blind vias extend through the metal layer on one side of the dielectric substrate and terminate into the metal layer formed on the other side of the dielectric substrate. Blind vias are typically formed using laser drilling or chemical etching techniques.

In high performance applications requiring dense circuit routing capability, a microvia structure is preferred. The microvia structure refers to circuits having via capture pads with diameters of 150 micrometers or smaller. In high performance applications, the via capture pad diameter is the critical design parameter for determining maximum circuit density rather than the via diameter. The capture pad diameter is the sum of the via diameter, the required fringe or "land" around the via, and the via to pad misalignment tolerance. Substrate distortion and via placement capabilities, both of which can be significant, contribute to defining the misalignment tolerance.

Capture pad diameters can be reduced by achieving a reduction in the via size, reducing substrate distortion, improving via placement or a combination thereof. Via size can be reduced through the use of sophisticated etching or laser drilling techniques. Reduction in distortion of the substrate can be achieved through the use of expensive and cumbersome apparatus, through the use of costly substrate processing measures, with an alternative substrate with specific dimensional stability properties, or a combination thereof. Consequently, typical techniques for reducing capture pad diameter typically add a considerable number of steps to conventional processes and substantially increase the cost of the resulting circuits.

Therefore, what is needed is a cost-effective process and resulting circuit construction providing reduced via size and reduced substrate distortion during processing.

Summary of the Invention

Accordingly, in one embodiment of the present invention, a printed circuit includes a dielectric substrate having two spaced apart major surfaces. A first conductive layer is formed on each major surface of the dielectric substrate. The dielectric substrate and the first conductive layers define a composite base substrate. A via including a sidewall extends through the composite base substrate. A conductive seed layer is formed on the sidewall of the via. A second conductive layer is formed contiguously on each one of the first conductive layers and on the conductive seed layer.

Vias according to the present invention preferably have a microvia construction. A microvia has a capture pad diameter less than 150 micrometers, a maximum via diameter less than 50 micrometers and a sidewall having a via taper angle less than 25 degrees.

The composite base substrate preferably has a tensile modulus at least 2 times greater than the tensile modulus of the dielectric substrate. Preferred materials for the dielectric substrate and for the conductive layers are polyimide film and copper, respectively.

Another embodiment of the present invention, a process for making a printed circuit includes providing a dielectric substrate having two spaced apart major surfaces and forming a first conductive layer on each one of the major surfaces of the

dielectric substrate. The dielectric substrate and the first conductive layers define a composite base substrate. A via including a sidewall is then formed through the composite base substrate and a conductive seed layer is formed on the sidewall of the via. Each first conductive layer is patterned to define a perimeter of a capture pad therein after the via is formed. Each capture pad encompasses the via and the perimeter of each capture pad having a diameter less than 150 micrometers. A contiguous second conductive layer is then formed on each one of the first conductive layers and on the conductive seed layer.

Formation of the via preferably includes the step of laser ablating through the composite base substrate. It is advantageous to form the via after forming the first conductive layers on the dielectric substrate. The composite base substrate exhibits significantly less distortion than does the dielectric substrate alone. Accordingly, reducing the distortion of the composite base substrate allows for precise positioning of the vias and capture pads and for reduced size of the capture pads.

Formation of the vias through the composite base substrate also allows the first conductive layer to act as a processing mask. The mask results in the vias having a smaller entrance side diameter and a smaller exit side diameter when formed using techniques such as laser ablation and chemical etching.

A unique aspect of processes according to the present invention is that laser ablation debris is removed during the step of forming a conductive seed layer on the side wall of the via. A plurality of steps are eliminated by structuring the process such that the web is cleaned during the via seeding operation. The via seeding operation is preferably accomplished using an chemical deposition method such as a direct metallization technique.

Formation of the contiguous second conductive layer preferably includes the step of simultaneously electroplating a layer of conductive material on the first conductive layer and on the seed layer of the via.

In a further embodiment of the present invention, a flexible circuit includes a flexible dielectric substrate having two spaced apart major surfaces. A first conductive layer is formed on each major surface of the dielectric substrate. The first conductive layers and the dielectric substrate define a composite base substrate having a tensile modulus at least 2 times greater than the tensile modulus of the dielectric substrate. A via including a sidewall extends through the composite base substrate.

The via defines edge portions in the composite base substrate. The edge portions of the via have respective diameters less than 50 micrometers and define a via taper angle less than 25 degrees. Each first conductive layer is patterned to define a perimeter of a capture pad encompassing the via. The perimeter of each capture pad has a diameter less than 150 micrometers. A conductive seed layer is formed on the sidewall of the via. A second conductive layer is formed contiguously on each first conductive layer and on the seed layer.

The following terms have the following meanings when used herein:

1. The term "composite base substrate" refers to a dielectric substrate having continuous conductive layers on at least one major surface thereof.

2. The term via refers to an aperture extending through the dielectric substrate and at least one conductive layer of the composite base substrate.

3. The term "direct metallization process" refers to a chemical process of forming a coating of electrically conductive material directly on a surface of a dielectric substrate, a layer of conductive material or both.

4. The terms "contiguous" and "contiguously" refers to a physically and electrically continuous manner in which a conductive layer extends from one major surface of a dielectric substrate to another major surface thereof through a via.

5. The term "laser ablation debris" refers to by-product portions of the dielectric substrate and conductive layers that are produced during the laser ablation process and that are deposited on a surface of the composite base substrate.

6. The term "edge portion" refers to a perimeter edge of the via at a respective surface of the composite base substrate.

7. The term "sidewall via taper angle" refers to the angle of the sidewall of the via relative to a reference axis extending perpendicular to the major surfaces of the composite base substrate.

8. The term "line-of sight" refers to a surface of a feature being visible from a particular position, such as, for example, the position of a plating material target in a sputtering deposition process.

Brief Description of the Drawings

Fig. 1 is a fragmentary plan view illustrating an embodiment of a circuit assembly including a plated through hole via having an open configuration.

Fig. 2 is a cross-sectional view taken along the line 2-2 in Figure 1.

Fig. 3 is a cross-sectional view illustrating an embodiment of a plated through hole via having a closed configuration.

Figs. 4A-4J are views illustrating an embodiment of a process for fabricating circuits according to the present invention.

Detailed Description of the Drawings

Circuit constructions according to the present invention provide a superior multi-metal layer circuit construction relative to conventional circuit constructions. Methods for fabricating circuits according to the present invention utilize a two-side metallized dielectric substrate. Preferably, the substrate is metallized with a seed layer of a conductive material such as copper. The metallized dielectric substrate is laser drilled to generate the desired pattern of vias. The metallized substrate exhibits greater resistance to distortion resulting from applied web tension and thermally induced stresses. Accordingly, microvias can be readily formed using such a substrate.

An embodiment of a circuit assembly 10 is illustrated in Figs. 1 and 2. The circuit assembly 10 includes a dielectric substrate 12 having a thickness t, a first major surface 12a and a second major surface 12b. A preferred material for the dielectric substrate 12 is a polyimide film such as that sold by DuPont under the tradename KAPTON E. Other suitable commercially available flexible polymeric films include, for example, Upilex™ offered by Ube and Apical™ offered by Kaneka.

The first major surface 12a extends generally parallel to the second major surface 12b. A first conductive layer 14 is formed on each one of the major surfaces 12a, 12b. The dielectric substrate 12 and the first conductive layers 14 define a composite base substrate 16, Fig. 2. As discussed below in reference to Figs. 4A-4J, each first conductive layer 14 preferably includes a base sputter layer, such as a layer of chromium, and a flash plate layer, such as a layer of copper. This first conductive layer 14 serves as an adhesive tie layer between the dielectric substrate 12 and subsequently formed conductive layers and as a plating bus for subsequently formed pattered conductive features. The first conductive layer 14 also adds enhanced stability of the composite substrate 16. One skilled in the relevant arts will

understand that the first conductive layer 14 can also be formed by other techniques such as vacuum metallization or electron beam evaporation.

A via 18 extends through the composite base substrate 16. The via 18 includes a sidewall 20 that extends through the composite base substrate 16. A seed layer 22 of electrically conductive material is formed on the sidewall 20 of the via 18. First and second edge portions 23a, 23b of the via 18 are defined at the intersections of the sidewall 20 and the first conductive layers 14. The first conductive layers 14 are patterned to define a perimeter of a capture pad 24 that encompasses the corresponding edge portions 23a, 23b and to define a perimeter of at least one trace 26 extending from the capture pad 24. A second conductive layer 28 is formed in a contiguous manner on the first conductive layers 14 and on the seed layer 22. The second conductive layer 28 is plated such that the via 18 has an open configuration wherein with an opening extends through the via 18.

The via 18 illustrated in Figs. 1 and 2 has a tapered sidewall profile. Vias having a tapered sidewall profile are typically produced using through hole fabrication methods such as, for example, laser ablation, laser drilling and chemical etching. As illustrated in Fig. 2, each one of these through hole fabrication methods produces a via 18 wherein the first edge portion 23a corresponding to an entry side of the through hole defines a first diameter D1 and wherein the second edge portion 23b corresponding to an exit side of the through hole defines a second diameter D2.

The first diameter D1 is greater than the second diameter D2. The first diameter D1 and the second diameter D2 define a via taper angle A. Through the use of preferred processing techniques, such as laser ablation, laser drilling and chemical etching, a via taper angle A of between 0 degrees and 60 degrees can be produced. The via taper angle A is defined herein according to the following equation.

$$A = \text{inverse tan } ((D1-D2)/2t)$$

For example, a via having a first diameter D1 of 50 microns, a second diameter D2 of 25 microns and a dielectric thickness t of 50 micros has a via taper angle A of 15 degrees.

An embodiment of a circuit assembly 110 is illustrated in Fig. 3. The circuit assembly 110 includes a dielectric substrate 112 having a via 118 extending therethrough. A first conductive layer 114 is formed on major surfaces 112a, 112b of

the dielectric substrate 112. The dielectric substrate 112 and the first conductive layers 114 define a composite base substrate 116. The via 118 has a sidewall 120 that extends in a direction substantially perpendicular to the major surfaces 112a, 112b of dielectric substrate 112. A seed layer 122 of electrically conductive material is formed on the sidewall 120 of the via 118. Typical through hole fabrication methods for forming non-tapered vias include, but are not limited to, mechanical punching and mechanical drilling.

The via 118 has a closed configuration, meaning that the through hole has been plated closed. This type of configuration is useful for preventing solder from draining from one side of a circuit to the another side thereof. The dimensions of the sidewall of a via and the thickness of the conductive layers dictate whether the via will have an open configuration (Fig. 1) or a closed configuration (Fig. 3). Decreasing the diameter of the via and increasing the thickness of the first and the second conductive layers will yield a closed via configuration. Increasing the diameter of the via or reducing the thickness of the first and the second conductive layers will yield an open via configuration.

An embodiment of a process for fabricating circuits according to the present invention is illustrated in figures 4A –4J. A dielectric substrate 200 has a base layer 202 formed on a first major surface 200a thereof and on a second major surface 200b thereof, Fig. 4A. It is preferred that the base layer 202 includes a tie layer, such as a layer of chromium, formed directly on the dielectric substrate 200 and a conductive seed layer, such as a layer of copper, formed on the tie layer. The base layers 202 enable plating and enhanced adhesion of subsequently formed conductive layers thereon. The tie layer serves as a diffusion barrier between the dielectric substrate and the conductive seed layer.

Sputtering is a preferred technique for forming the base layer 202. Other techniques for forming the base layer 202 include other chemical deposition techniques such as chemical vapor deposition. Typically, the base layer 202 is formed on the first surface 200a and then on the second surface 200b. However, depending on the specific application and processing equipment, other sequences for forming the base layers 202 may be applicable.

In a typical sputtering operation, the dielectric substrate 200 is subjected to an infrared preheating operation to remove moisture. Following the preheat step, the

first and second surfaces 200a, 200b of the dielectric substrate 200 are exposed to an oxygen plasma for preconditioning the surfaces 200a, 200b. The first surface 200a of the dielectric substrate 200 is then subjected to a tie layer sputter operation and then to a seed layer sputter operation, forming the base layer 202 on the first surface 200a. Following formation of the base layer 202 on the first surface 200a, the same operations are repeated on the second surface 200b to form the base layer 202 thereon.

A typical thickness for the tie layer and for the seed layer on the first surface 200a is 70 angstroms and 150 nm, respectively. During formation of the first conductive layer 202 on the second surface 200b, the plasma and sputter energies may be maintained at levels about 10% lower than those used on the first surface 200a, reducing heating and distortion of the dielectric substrate 200. A typical thickness for the tie layer and for the seed layer on the second surface 200b of the dielectric substrate 200 is 70 angstroms and 130 nm, respectively. A plurality of suitable plasma and sputtering processes and process equipment are known in the circuit fabricating industry. Preferred process equipment will have a plurality of deposition zones such that the tie layer and the seed layer can be formed in a single pass through the process equipment.

Following formation of the base layers 202 on the dielectric substrate 200, a flash plate layer 204, Fig. 4B, is formed on each one of the base layers 202. Each base layer 202 and the adjacent flash plate layer 204 define a first conductive layer 205. Electroplating is a preferred plating technique for forming the flash plate layer 204. The flash plate layers 204 are preferably formed simultaneously to reduce the total number of processing steps. A target thickness for each flash plate layer 204 is 3 μm. However, the thickness of the flash plate layers 204 may vary depending on the specific application. A plurality of suitable electroplating processes and process equipment are known in the circuit fabricating industry.

The dielectric substrate 200, the base layers 202 and the flash plate layers 204 define a composite base substrate 206, Fig. 4C. The composite base substrate 206 preferably exhibits a composite tensile modulus at least 2 times greater than the tensile modulus of the dielectric substrate 200. By achieving such a composite tensile modulus, distortion of the composite base substrate 206 is substantially reduced during subsequent processing operations.

After formation of the flash plate layers 204, one or more vias 208 are formed through the composite base substrate 206, Fig. 4C. Commercially available methods for forming the one or more vias 208 include methods such as laser ablation, laser drilling, mechanical drilling, mechanical punching and chemical milling. Laser ablation is a preferred method of forming the one or more vias 208.

In one embodiment of a laser ablation method, a commercially available laser system is used for forming the one or more vias 208. A suitable laser system is offered by Electro Scientific Industries, Incorporated (ESI) under the model number 5200. U.S. Patent number 5,593,606 issued to ESI discloses a suitable method for using a laser to laser ablate apertures such as vias in materials such as the dielectric substrate 200.

The one or more vias 208 are formed through the composite base substrate 206 from an entry side 206a to an exit side 206b, Fig. 4C. Formation of the one or more vias 208 through the composite base substrate 206 is known to deposit laser ablation debris 210 on the entry side 206a of the composite base substrate 206 and to form a rim portion 212 on the exit side 206b of the composite base substrate 206. The laser ablation debris 210 and rim portion 212 are preferably removed from the composite base substrate 206 during the following process steps.

Next, a seed layer 214 is formed on a sidewall 216 of each one of the vias 208, Fig. 4D. A deposition process known as "direct metallization" is a preferred process for forming the seed layer 214. Direct metallization is a process technique in which a non-conductive surface can be directly electroplated without first having to form a conductive layer thereon. Direct metallization involves coating of a surface with a conductive material, allowing the surface to be subsequently electroplated. The direct metallization process may be facilitated using commercially available process equipment from suppliers such as Finishing Services, Western Technology Associates, Schmid and Atotech.

Suitable commercially available direct metallization process and chemistry include carbon-based systems such as those offered by Electrochemicals Incorporated under the tradename Shadow Direct Metallization, by McDermid under the tradename BlackHole and by Shipley-LeaRonal under the tradename Graphite 2000; Pd-Colloid chemistries such as those offered by Atotech under the tradename Neopact and by Solution Technology Systems under the designation HN504; and conductive polymer

systems such as that offered by Atotech under the tradename Compact CP. Any of these direct metallization processes and chemistries or suitable known chemical copper deposition techniques can be used to form the seed layer on the sidewall 216 of the one or more vias 208.

A key benefit of direct metallization processes is the ability to form a conductive seed layer on vias having high aspect ratios because this type of metallization process is not line-of-sight limited. Because direct metallization processes are predominately based on wetting or viscosity characteristics of the direct metallization solution, forming a seed layer on difficult to reach locations is directly related to the ability to expose such locations to the direct metallization plating solutions. Providing that the proper chemistry of the plating solution is maintained, the plated layer of material resulting from the direct metallization process will be relatively uniform on all exposed surfaces of the article being plated.

Another key benefit of direct metallization is that the laser ablation debris 210, Fig. 4C, is removed during the direct metallization process.

Other desirable attributes of direct metallization processes include ease of processing; relatively low-cost processing; relatively low sensitivity to contamination and to copper brightening systems; not requiring high current densities to initiate and plate; and relatively low rinse water consumption, analysis time, equipment power consumption and waste treatment costs.

Metallization techniques such as sputtering and evaporation are line-of-sight. The uniformity of the resulting layer of material is dependent on the orientation of the substrate and features therein. The relative coating rate between the side walls of a via and the flat surface of a substrate is related to two ratios: (1) via diameter/via depth and (2) via diameter/molecular mean free path. If the mean free path is much less that of the diameter, then the resulting coating will be uniform. If the mean free path is greater than or slightly equal to the diameter, then the coating rate is a strong function of via depth. In most vacuum processes, the mean free path is typically greater than 100 micrometers. (This means it will be difficult to uniformly coat a 25 micrometer diameter via.) Accordingly, it is difficult and costly to form a relatively uniform seed layer on vias having vertical or nearly vertical sidewalls relative to the major surfaces of the substrate.

An embodiment of a direct metallization process includes a first operation of conditioning the composite base substrate 206 in a mildly alkaline solution. The alkaline solution cleans and conditions the substrate surfaces 206, including sidewall 216. Loosely adhered portions of the laser ablation debris 210 are removed during conditioning of the composite base substrate 206.

The conditioning agents present in the alkaline solution form strong cationic charges on the exposed surfaces of the composite base substrate 206. These charges remain intact through the conditioner operation and through subsequent rinse, allowing for the attraction and attachment of seeding material.

The direct metallization process uses a metallization solution comprised of a mildly alkaline conductive colloid dispersion formulated from bound graphite. Graphite, together with an organic binder exists as an anionic charged particle which is very attracted to the cationic charge left on the sidewall 216 of the via 208 during the conditioner step. The composite base substrate 206 is immersed in the metallization solution such that the seed layer 214 is formed on the sidewall 216 of each via 208, Fig. 4D, and on the exposed portions of the flash plate layers 204.

When carbon deposits need to be removed from copper surfaces, the composite base substrate 206 is subjected to an acidic fixer solution which removes excess graphite colloid. Exposure to the fixer solution promotes better adhesion from the remaining, tightly bound seed layer 214. The fixer solution acts to neutralize and crosslink the carboxyl groups on the binder, causing the graphite particles to flocculate onto the sidewall 216 and reducing the amount of graphite that turns to precipitate. A rinse water step directly after exposure to the fixer solution removes any graphite precipitate.

The seed layer 214 is then dried to prevent it from being washed off in subsequent operations. Heat applied during the drying operation completes the crosslinking of the seed layer 214.

The portions (not shown) of the seed layer 214 deposited on the flash plate layers 204 are removed during a subsequent micro-etch operation. The seed layer 214 on the exposed portions of the flash plate layers 204 is removed using a persulfate etchant. If the flash plate layer 204 is made of copper, the persulfate penetrates the seed layer 214 on the flash plate layer 204 and begins to etch the copper away, carrying the graphite with it. The persulfate does not react with polymeric substrates.

Accordingly, the seed layer 214 remains intact on the sidewall 216 of each via 208. Well adhered portions of the laser ablation debris 210, Fig. 4C, are removed during micro etching operation.

Following the formation of the seed layer 214 on the sidewall 216 of each via 208, Fig. 4D, a photoresist layer 218 is formed on each flash plate layer 204, Fig. 4E. Each photoresist layer 218 is preferably an aqueous processible, dry-film, negative-acting photoresist applied using heat and pressure. The thickness of each photoresist layer 218 is typically between 15 micrometers and 50 micrometers. Suitable photoresists for each photoresist layer 218 include, for example, photoresists offered by MacDermid Incorporated under the series designations SF, CF, and MP. Specific examples include MacDermid SF310 and MP413 photoresists.

After lamination of the photoresist layers 218, a suitable photomask 220 is engaged against each photoresist layer 218, Fig. 4F. Each photomask 220 includes a pattern that is registered with respective portions of the corresponding flash plate layer 204 and dielectric substrate 200. Commercially available equipment, such as that available from Perkin Elmer-ORC, is used to register each photomask 220 with respective portions of the corresponding flash plate layer 204 and dielectric substrate 200. The photoresist layers 218 are then exposed to energy from a suitable source for exposing a desired image in the photoresist layer 206. An ultraviolet light source 222 is commonly used for exposing images in photoimageable photoresists, such as the photoresist layers 218. Other commercially available exposure equipment is offered by companies such as Tamarac, Ushio, and Siposa SA.

The photomasks 220 include patterned chrome or emulsion coated portions for blocking the transmission of energy to specific areas of the photoresist layers 218, allowing energy to pass through and react with the photoresist layer 218 in unblocked areas. Preferably, the photo resist layers 218 are imaged simultaneously, reducing the number of process steps and improving registration. Photomasks of various constructions are commercially available.

Following exposure of the photoresist layers 218, areas of the photoresist layers 218 that were not exposed to energy are developed in a suitable developing solution, Fig. 4G. In a preferred embodiment where each photoresist layer 218 is an aqueous negative-acting material, the areas of each photoresist layer 218 that were not exposed to energy from the light source 222 are developed out (removed) during the

developing step. In the case of aqueous processible photoresists, the developing step includes applying a dilute aqueous solution, such as a 0.5% - 1.5% sodium or potassium carbonate solution, to the photoresist until the desired patterns are obtained in the photoresist layers 218.

The developing step is typically performed using commercially available equipment and solutions. The developing step results in a desired circuit pattern in the photoresist layer 206, Fig. 4G. The pattern includes portions exposing the flash plate layers 204 and the vias 208.

Next, the sidewall 216 of each via 208 and the portions of the flash plated layer 204 exposed through the photoresist layers 218 are simultaneously plated with a layer of conductive material, Fig. 4H. The layer of conductive material forms a contiguous second conductive layer 224 on the first conductive layers 205 and on the seed layer 214 of each via 208. A typical combined thickness for the first and second conductive layers 205, 224 is 15 μm. However, the specific thickness may be different for a particular circuit design.

A key aspect of the present invention is that the second conductive layer 224 is simultaneously formed on the first conductive layers 205 and on the seed layer 214 of each via 208. Simultaneously plating of the second conductive layer 224 eliminates additional process steps that are required with a multiple pass plating operation. Furthermore, the resulting contiguous second conductive layer 224 provides improved resistance to corrosion and stress related failures.

The photoresist layers 218 are then stripped off both sides of the composite base substrate 206, Figs. 4H and 4I. A suitable method for stripping the photoresist layers 218 comprises exposing the photoresist layers 218 to a solution (typically 2 - 10%) of an alkaline metal hydroxide at from 20°C to 80°C, preferably from 20°C to 60°C. Stripping the photoresist layers 218 exposes portions of the first conductive layer 205 that were previously concealed by the photoresist layers 218.

Lastly, the portions of the first conductive layer 205 that were previously concealed by the photoresist layers 218 are etched away to form electrically isolated capture pad portions 226 encompassing each via 208 and traces 228, Fig. 4J. Suitable methods are known in the art for etching the first conductive layers 205.

There are many benefits according to the present invention. One benefit is that the via and circuit are formed after the dielectric has been dimensionally

stabilized through a metallization process. The metallization process enables superior via to capture pad alignment. This improved alignment in conjunction with the small diameter vias produced using a laser process, such as laser ablation, results in reduced capture pad diameters and higher circuits densities. Another benefit is that simultaneous two-sided plating of the circuitry and via is used to provide a via construction with significantly reduced corrosion and stress related reliability concerns. A further advantage is a reduction in the number of processing steps that are required. Conventional methods for producing two side metallized substrates with plated vias require at least 2 times the number of processing steps utilized for a single metal circuit. In accordance with the present invention, a process is achieved that uses only 1.5 times the number of steps utilized in a single metal circuit. Process techniques such as simultaneous two-side patterning, direct metallization of the via and simultaneous plating of all conductive features of a circuit results in a reduced number of process steps. Processes according to the present invention enable the fabrication of lower cost two metal layer circuits that offer enhanced reliability, reduced capture pad diameter and higher via density.

Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the embodiments and descriptions disclosed herein.

What is claimed is:

1. A printed circuit, comprising:

a dielectric substrate having two spaced apart major surfaces;

at least one first conductive layer formed on each major surface of the dielectric substrate, the dielectric substrate and the first conductive layers defining a composite base substrate;

at least one via including a sidewall extending through the composite base substrate;

a conductive seed layer formed on the sidewall of the via; and

a second conductive layer formed contiguously on each one of the first conductive layers and on the conductive seed layer;

wherein the composite base substrate has a tensile modulus at least 2 times greater than the tensile modulus of the dielectric substrate.

2. A flexible printed circuit, comprising:

a flexible dielectric substrate having two spaced apart major surfaces;

a first conductive layer formed on each major surface of the dielectric substrate, the first conductive layers and the dielectric substrate defining a composite base substrate having a tensile modulus at least 2 times greater than the tensile modulus of the dielectric substrate;

a via including a sidewall extending through the composite base substrate, the via defining edge portions in the composite base substrate, the edge portions of the via having respective diameters less than 50 micrometers and defining a via taper angle less than 25 degrees, each first conductive layer patterned to define a perimeter of a capture pad encompassing the via, the perimeter of each capture pad having a diameter less than 150 micrometers; a conductive seed layer formed on the sidewall of the via; and

a second conductive layer formed contiguously on each first conductive layer and on the seed layer.

3. A printed circuit according to claim 1 or 2 wherein each first conductive layer is patterned to define a perimeter of a respective capture pad therein,

each capture pad encompassing the via, wherein the perimeter of each capture pad has a diameter less than 150 micrometers.

4. A printed circuit according to claim 3 wherein the sidewall of the via has a via taper angle less than 25 degrees.

5. A printed circuit according to claim 3 wherein the via defines edge portions in the composite base substrate, each edge portion of the via having a respective diameter less than 50 micrometers.

6. A printed circuit according to claim 1 or 2 wherein the dielectric substrate is a polyimide film and wherein the first conductive layer is formed from copper having a thickness of less than 3 micrometers.

7. A printed circuit according to claim 1 or 2 wherein the dielectric substrate has an tensile modulus of less than $1x10^6$ psi, and a thickness of less than 25 micrometers.

8. A printed circuit according to claim 1 or 2, made by a process comprising the steps of:

forming the first conductive layer on each one of the major surfaces of the dielectric substrate;

forming the via through the composite base substrate;

forming the conductive seed layer on the sidewall of the via; and

simultaneously forming the second conductive layer on each one of the first conductive layers and on the conductive seed layer.

9. The printed circuit of claim 8 wherein the step of forming the via includes the step of laser ablating through the composite base substrate and the first conductive layer.

10. The printed circuit of claim 8 wherein the step of forming the conductive seed layer on the sidewall of the via includes the steps of chemically depositing a seed layer coating on the sidewall of the via and concurrently removing laser ablation debris from the composite base substrate.

12. The printed circuit of claim 8 wherein the step of forming the conductive seed layer includes the steps of:

conditioning the sidewall of the via for receiving a seed layer coating thereon and for removing loosely adhered laser ablation debris from the composite base substrate; and

etching the composite base substrate for removing a residual seed layer coating from the first conductive layers and for removing well adhered laser ablation debris from the composite base substrate.

13. The printed circuit of claim 8 wherein the step of forming each first conductive layer includes the steps of forming a tie layer on each major surface of the dielectric substrate and then forming a flash plate layer on each tie layer.

14. The printed circuit of claim 8 wherein the step of forming the second conductive layer includes the step of simultaneously electroplating a layer of conductive material on the first conductive layers and on the conductive seed layer.

15. The printed circuit of claim 8, further comprising the step of:

patterning each first conductive layer to define the perimeter of a capture pad therein after the via is formed, each capture pad encompassing the via.

16. The printed circuit of claim 15 wherein the step of patterning the first conductive layers includes the steps of forming a photoresist layer on each first conductive layer, forming an opening extending through each photoresist layer wherein a portion of each first conductive layer is exposed through the opening in the respective photoresist layer, and etching each first conductive layer through the opening in the respective photoresist layer.

17. A printed circuit according to claim 1 or two made by a process comprising the steps of:

providing a dielectric substrate having two spaced apart major surfaces;

forming a first conductive layer on each one of the major surfaces of the dielectric substrate wherein a composite base substrate is defined by the dielectric substrate and the first conductive layers;

forming a via including a sidewall through the composite base substrate;

forming a conductive seed layer on the sidewall of the via;

patterning each first conductive layer to define a perimeter of a capture pad therein after the via is formed, each capture pad encompassing the via and the perimeter of each capture pad having a diameter less than 150 micrometers; and

forming a contiguous second conductive layer on each one of the first conductive layers and on the conductive seed layer.

18. The process of claim 17 wherein the step of forming the conductive seed layer on the sidewall includes the steps of chemically depositing a seed layer coating on the sidewall of the via and concurrently removing laser ablation debris from the composite base substrate.

19. The process of claim 17 wherein the steps of forming the conductive seed layer includes the steps of:

conditioning the sidewall of the via for receiving a seed layer coating thereon and for removing loosely adhered laser ablation debris from the composite base substrate; and

etching the composite base substrate for removing the layer a residual seed layer coating from the first conductive layers and for removing well adhered laser ablation debris from the composite base substrate.

20. The process of claim 17 wherein the step of forming the conductive seed layer on the sidewall of the via includes the step of performing a direct metallization operation for forming a seed layer coating directly on the sidewall of the via.

21. The process of claim 20 wherein the step of performing the direct metallization operation includes the steps of forming the seed layer coating on the sidewall of the via and cleaning laser ablation debris from a surface of the composite base substrate.

22. The process of claim 17 wherein the step of forming each first conductive layer includes the steps of forming a tie layer on each major surface of the dielectric substrate and then forming a flash plate layer on each tie layer.

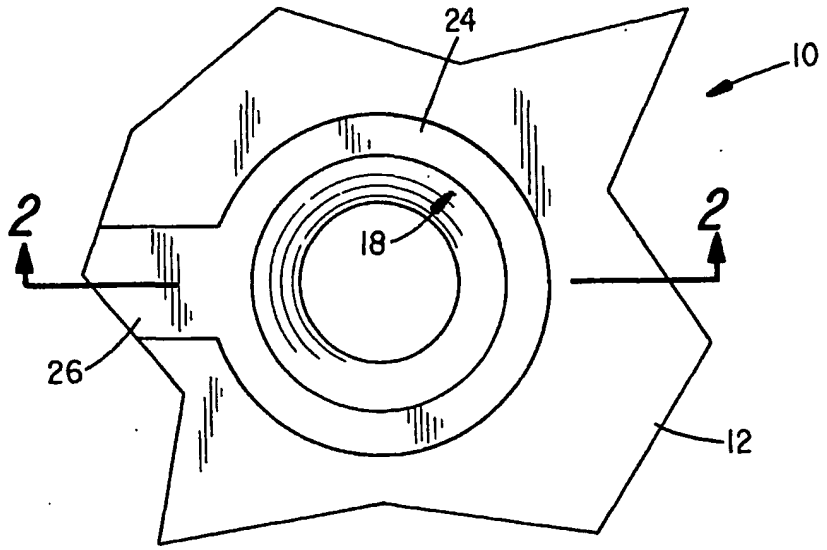
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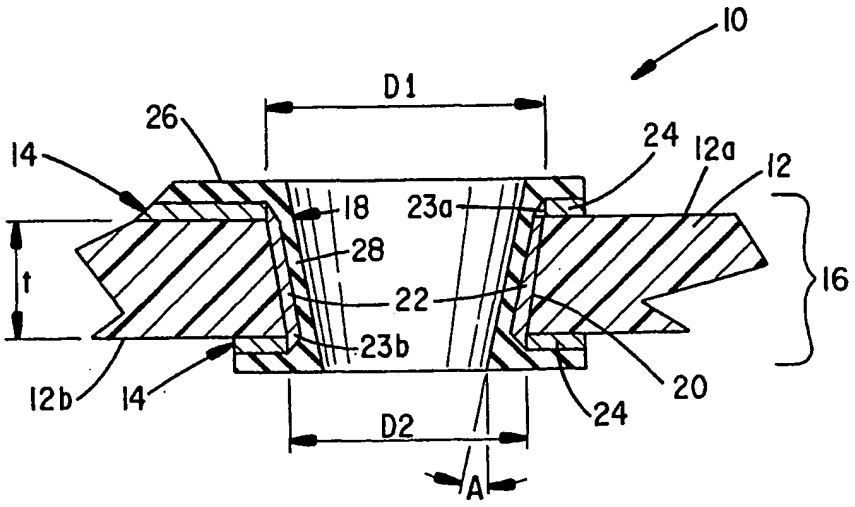
FIG. 1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D2
A

FIG. 2

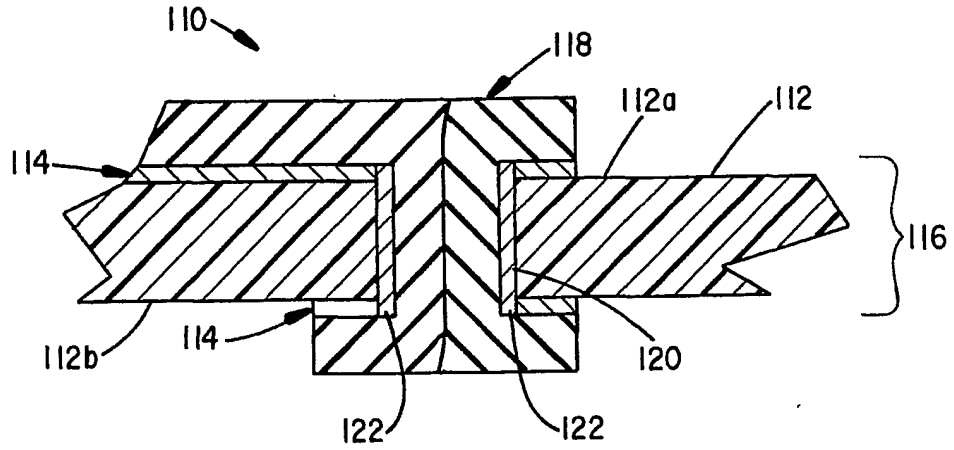

FIG. 3

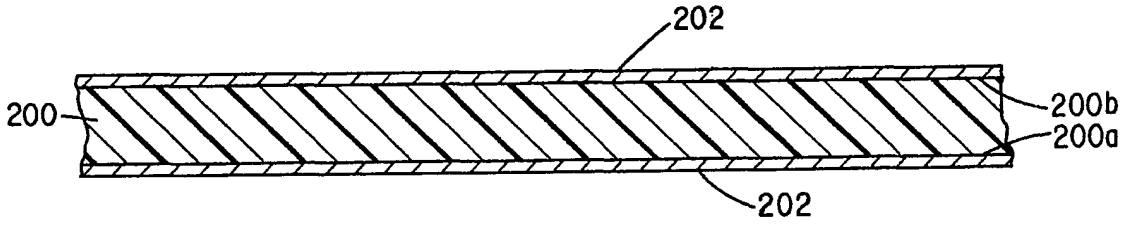

FIG. 4A

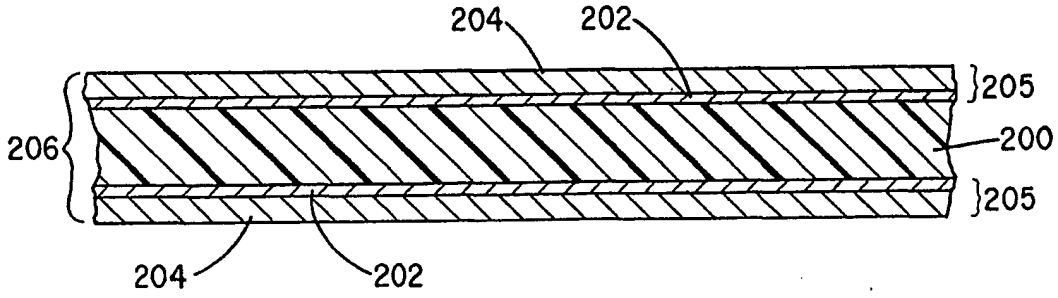

FIG. 4B

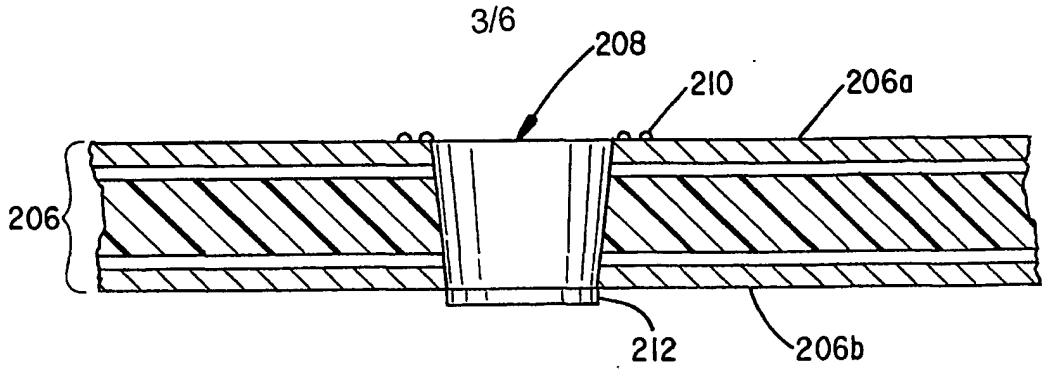

FIG. 4C

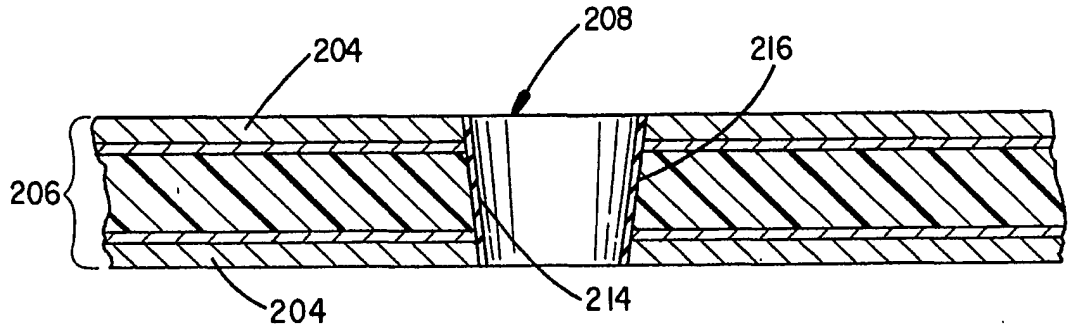

FIG. 4D

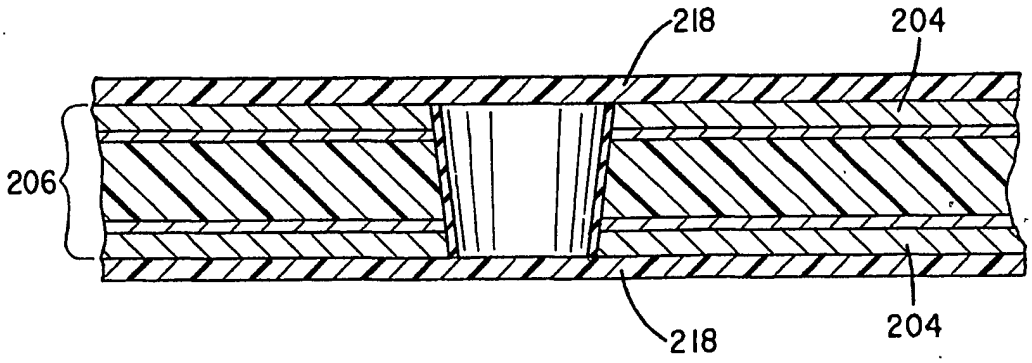

FIG. 4E

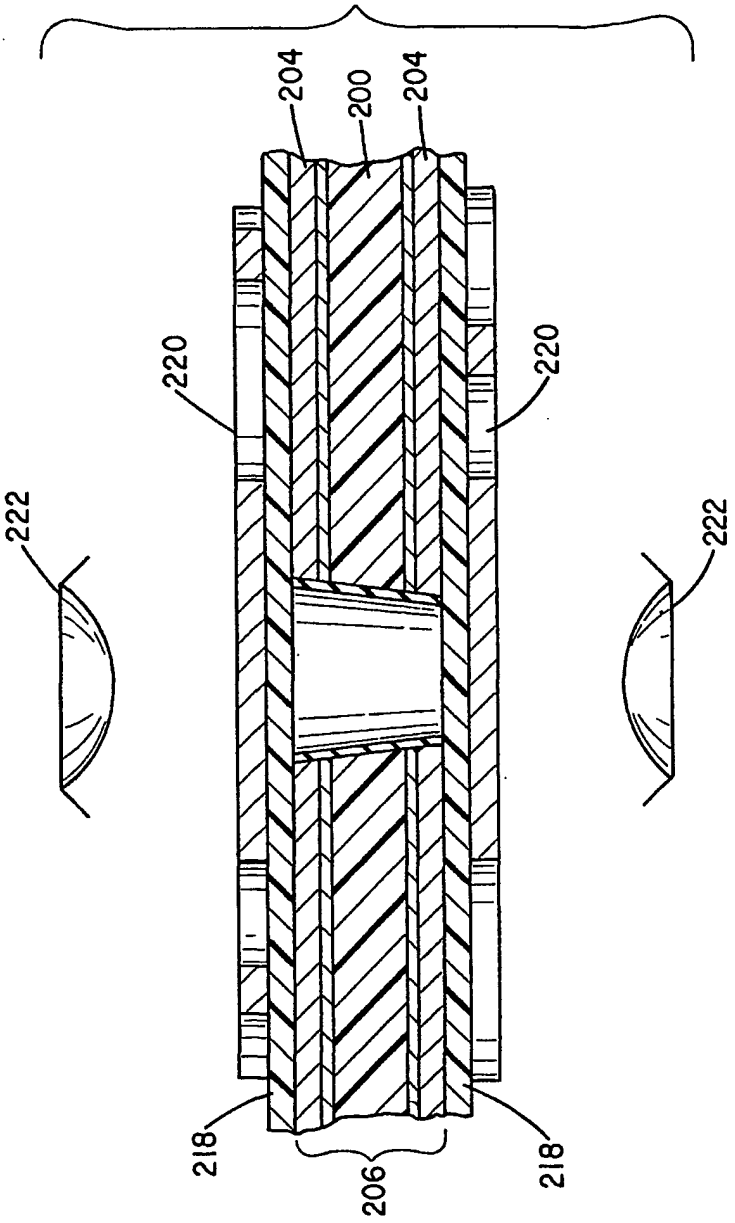

FIG. 4F

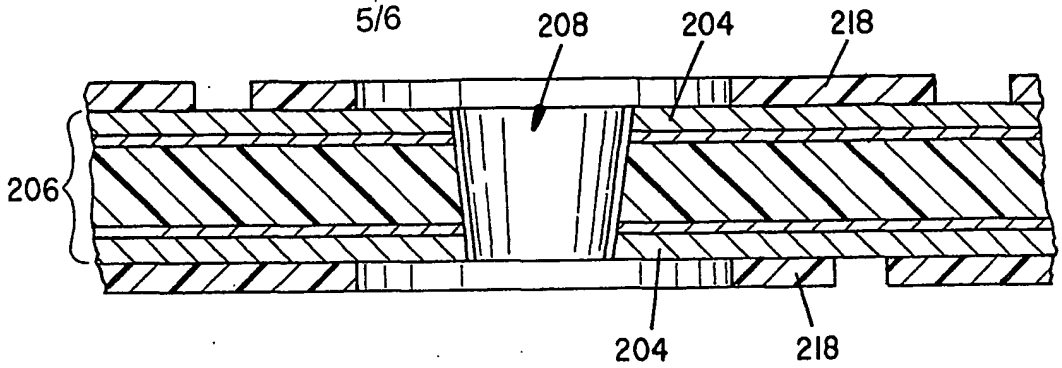
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FIG. 4G

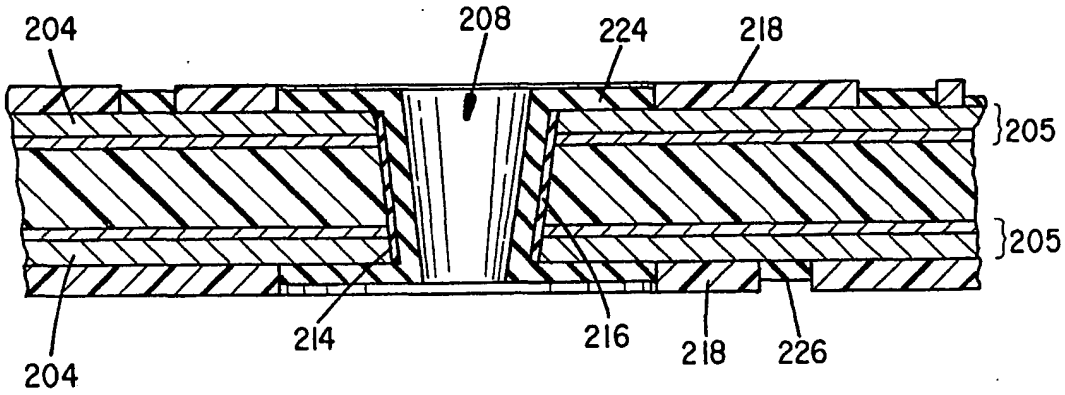
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FIG. 4H

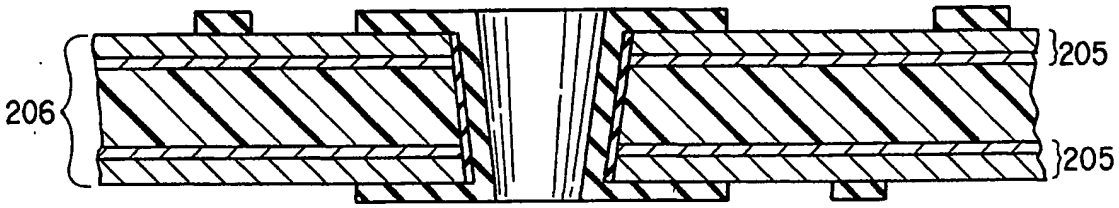

FIG. 4I

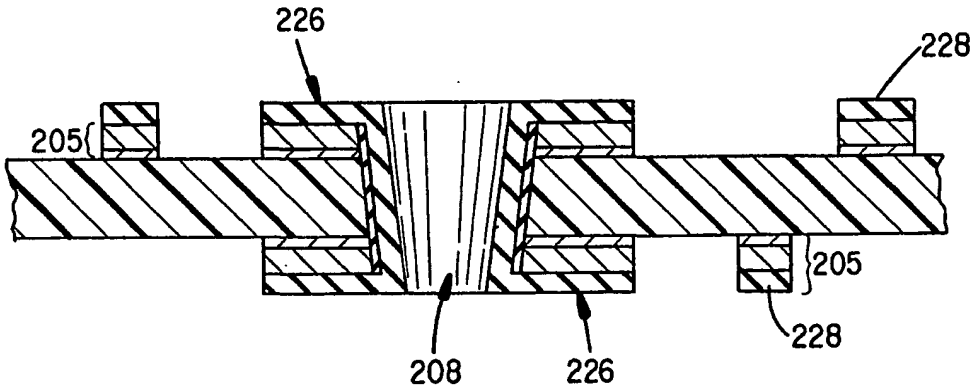

FIG. 4J

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/30007

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K3/42 H05K3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 039 889 A (ZHANG ET AL.) 21 March 2000 (2000-03-21) column 4, line 53 -column 5, line 47; figure 2	1-6, 8-10, 14-18, 20,21
Y	---	7,13,22
A	EP 0 257 737 A (MINNESOTA MINING & MFG CO) 2 March 1988 (1988-03-02) column 3, line 52 -column 5, line 47; figure 2	6
Y	---	7,13,22
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 January 2001	08/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Mes, L

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 108 553 A (FOSTER ET AL.) 28 April 1992 (1992-04-28) column 6, line 57 - line 64 column 8, line 8 - line 47 column 10, line 50 -column 11, line 45 column 12, line 26 - line 32 figures	1-6, 8-10,12, 14-21
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 09, 30 July 1999 (1999-07-30) & JP 11 097491 A (SHINDO DENSHI KOGYO KK), 9 April 1999 (1999-04-09) abstract	1,2,6, 8-10, 14-18,20
A	"COMBINED LASER PROCESSING OF VIAS AND CIRCUITRY IN FLEX-CIRCUITS" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 38, no. 5, 1 May 1995 (1995-05-01), pages 607-608, XP000519699 ISSN: 0018-8689 the whole document	1,2,4-6, 8,9,14, 17
A	"STRUCTURING OF LAMINATED CU-POLYIMIDE FILMS VIA LASER ABLATION" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 37, no. 8, 1 August 1994 (1994-08-01), page 481 XP000456496 ISSN: 0018-8689 the whole document	1,2,8,9

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/30007

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6039889 A	21-03-2000	JP 2000208901 A	28-07-2000
EP 0257737 A	02-03-1988	CA 1263763 A	05-12-1989
		JP 1773034 C	14-07-1993
		JP 4065558 B	20-10-1992
		JP 62293689 A	21-12-1987
		KR 9601355 B	26-01-1996
US 5108553 A	28-04-1992	US 5065228 A	12-11-1991
		AU 5330390 A	05-11-1990
		WO 9012422 A	18-10-1990
JP 11097491 A	09-04-1999	JP 3034829 B	17-04-2000